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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,290	06/28/2001	Jonathan Westphal	52254-016	6488

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/787,290	WESTPHAL, JONATHAN	
	Examiner	Art Unit	
	William D. Thomson	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005 and 08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 remain in the case.

2. Claims 1-12 have been once rejected in the Office Action dated June 04, 2004.

3. Applicant's filing of a Notice of Appeal, dated June 29, 2005, is now moot based upon the following:

   a. Withdrawal of the finality of the last rejection

   b. The office action dated February 25, 2005 is herby vacated.

4. Examiner has interpreted Applicant's after final amendment with remarks as a request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. Moreover, the February 25, 2005, Office Action is vacated.

The following is a complete explanation of the Examiner's reasoning as to why the finality has been removed, the last office action vacated, and that the Applicant's responses have been held either non-responsive or premature in their nature.

The reply filed on November 8th, 2004 was not fully responsive to the prior Office Action of June 2004, because of the following omission(s) or matter(s):

A review of the record shows only one set of claims that where originally filed in the 371 case. A copy of these claims have been attached to this action as Exhibit A.

A further review of the record shows a separate set of claims, Exhibit B, different from those in the pending case, Exhibit A claims, were filed with the November 8, 2004 response. These are not identical to the claims pending in the instant case. A copy of these new claims have been attached to this action as Exhibit B.

Per Applicant's arguments regarding the rejections and objections to the claims, the set presented in the November 8th, 2004 do not have a number of the issues raised in the first office action. For example, looking at the operation in step g1 which includes "as in figure 14" and "for I-point then 6", the pending claims include this language, whereas the claims presented with the November 8th, 2004 response do not have this language. The problem is that the Examiner now has two differing sets of claims before him without an amendment aligning the two.

A review of the record does not show a preliminary amendment after the filing of the 371 case as a U.S. filing. Therefore the claims presented on November 8th, 2004 are not presently in front of the Office.

Another problem is that in the November 8th, 2004 response, the Applicant characterized these issues as "certain informalities", whereas these are issues raised under a 35 U.S.C. 112 2nd paragraph rejection since the claims were, as presented, omnibus, did not provide antecedence and indefinite language including "i.e" and "such as".

The Examiner was anticipating a response with amendments correcting and cleaning up the claim language, since they were "narrative in form and replete with indefinite and functional or operational language. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device. The claim must be in one sentence form only. Note the format of the claims in the patent cited."

The Examiner that prosecuted the Final Office action, not the undersigned, did not notice that the claims were in fact different and the amendments did not completely resolve the issues under 35 U.S.C. 112 2nd paragraph.

Because of these issues the Primary Examiner has reopened the prosecution, removed the finality of the last rejection, vacated the last rejection and is providing the Applicant with the opportunity to provide a complete response that will clarify the record.

A complete response should include:

1- an amendment to the claims, see Exhibit A, that brings them into alignment with claims in Exhibit B, with amendments clean up any informalities.

2- amendments that resolve the use of indefinite language of "such as" and the use of "i.e."

3- include the amendments to the Abstract and specification as provided in the after final amendments dated June 29, 2005.

4- providing a copy of the references cited in the Applicant's specification so that the examiner may determine if they are essential or material to the case. This is not a formal requirement under 37 C.F.R. 1.105, however, not providing these materials may precipitate one.

5. See 37 CFR 1.111. Since the above-mentioned reply appears to be *bona fide*, applicant is given **ONE (1) MONTH or THIRTY (30) DAYS** from the mailing date of this

notice, whichever is longer, within which to supply the omission or correction in order to avoid abandonment. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

CONTACT INFORMATION

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William D. Thomson whose telephone number is 571-272-3718. The examiner can normally be reached on 8:30-3:30 Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William Thomson
Primary Examiner
Technology Center 2100
Art Unit 2123

EXHIBIT A

Claims:

1. A method of designing logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit to be designed as points and vectors in a vector space; and
   b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and
   c. designing the logical circuit using the simpler form.

2. A method of manufacturing logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit to be manufactured as points and vectors in a vector space; and
   b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and
   c. using the simpler form to implement the logical circuit in hardware.

3. A method of simplifying logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit as points and vectors in a vector space; and
   b. modifying the representation in vector space using at least one process rule of a set of process rules to simplify the logic.

4. The method of claim 3 in which at least one process rule of a set of process rules consisting of the following process rules:
   a. Process Rule 1--
      a1. Represent the alternational normal schema, the target schema t, as a set of vectors in the ANS-space,

      a2. Each clause or disjunct of t is a position vector (i.e. one pointing to O) with O at one corner of a set of parallelograms made of propositional addresses to the i-point at the other,

      a3. Any two other outside vertices of such a parallelogram are implicants which are among the original clauses of t;

   b. Process Rule 2--
      b1. Pick any two clauses,
      b2. If there is a propositional address σ at the midpoint between the component clauses, the vector from i to σ, i.e. σ, is the simplification of and can replace the relevant clauses of t, as in the case where t is $pq \vee p\bar{q}$, i is pp and σ is p;
   c. Process Rule 3--
      c1. Generate i-implicants until each clause or vector has been used at least once,

c2. If a disjunct **d** of **t** cannot be used because it forms no propositional address with any other disjunct, then **d** must appear unmodified in the final schema which is the simplification of **t**;

d. Process Rule 4--
d1. If an **i**-point exists in **t**, delete the vectors which produce it in favor of the vector from **i** to **O**;

e. Process Rule 5--
e1. For a clause in a schema which subsumes another clause eliminate the subsuming clause;

f. Process Rule 6--

f1. Couples such as **pq** v $\bar{p}\,\bar{q}$ or $\bar{p}\,\bar{q}s$ v **pq**$\bar{s}$ cannot be summed to zero; the origin.

g. Process Rule 7--

g1. Translate vectors as in Figure 14 if a corresponding σ-point exist for a i-point then 6 is the simplification of **i**.

g2. Any superpositions of parallel arrows in opposite directions represent equivalences,

g3. For equivalences, (a) Drop the longer clause at either end of any double-headed arrow, (b) Drop pairs, triples etc. of double-headed arrows which meet at a point in favor of the vector from that point to **O** and (c) Drop a vector or clause in the target schema which is itself the resultant of any other two vectors;

h. Process rule 8--

h1. A simplification is complete if in the system which replaces the target schema no vectors or clauses are subsumed by others and no double-headed vectors remain (i.e. if all equivalences in the system have been exploited).

5. Apparatus for simplifying logical circuits, comprising:
   a. a processing element configured to represent the logic of a logical circuit to be simplified as points and vectors in a vector space and to use the points and vectors to simplify the logic of the logical circuit to a simpler form.

6. The apparatus of claim 5 in which the processing element is an optical computer.
7. The apparatus of claim 5 in which the processing element is a digital computer.

8. The apparatus of claim 1 in which the processing element is an colorimetric computer.
9. The apparatus of claim 1 in which the processing element is an analog computer.
10. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be designed as points and vectors in a vector space and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form and for designing the logical circuit using the simpler form.

11. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be manufactured as points and vectors in a vector space, and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form, and for using the simpler form to implement the logical circuit in hardware.

12. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit as points and vectors in a vector space, and for modifying the representation in a vector space using at least one process rule of a set of process rules to simplify the logic.

EXHIBIT B

In re Patent Application of:
WESTPHAL
Serial No. **09/787,290**
Filed: **JUNE 28, 2001**
_____/

In the Claims:

Please amend the above-identified application as follows:

Claim 1 (original) A method of designing logical circuits, comprising the steps of:

a. representing the logic of a logical circuit to be designed as points and vectors in a vector space; and

b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and

c. designing the logical circuit using the simpler form.

Claim 2 (original) A method of manufacturing logical circuits, comprising the steps of:

a. representing the logic of a logical circuit to be manufactured as points and vectors in a vector space; and

b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and

c. using the simpler form to implement the logical circuit in hardware.

Claim 3 (original) A method of simplifying logical circuits, comprising the steps of:

a. representing the logic of a logical circuit as points and vectors in a vector space; and

b. modifying the representation in vector space using at least one process rule of a set of process rules to simplify the logic.

Claim 4 (currently amended) The method of claim 3 in which at least one process rule of a set of process rules consists of one of the following process rules:

a. Process Rule 1--

a1. Represent the alternational normal schema, the target schema **t**, as a set of vectors in the ANS-space,

a2. Each clause or disjunct of **t** is a position vector (i.e. one pointing to **O**) with **O** at one corner of a set of parallelograms made of propositional addresses to the ι-point at the other,

a3. Any two other outside vertices of such a parallelogram are implicants which are among the original clauses of **t**;

b. Process Rule 2—

b1. Pick any two clauses,

b2. If there is a propositional address σ at the midpoint between the component clauses, the vector from ι to σ, is the simplification of and can replace the relevant clauses of **t**;

c. Process Rule 3—

c1. Generate ι implicants until each clause or vector has been used at least once,

c2. If a disjunct **d** of **t** cannot be used because it forms no propositional address with any other disjunct, then **d** must appear unmodified in the final schema which is the simplification of **t**;

d. Process Rule 4—

d1. If an ι point exists in **t**, delete the vectors which produce it in favor of the vector from ι to **O**;

e. Process Rule 5—

e1. For a clause in a schema which subsumes another clause eliminate the subsuming clause;

f. Process Rule 6—

f1. Couples such as **pq v** $\bar{p}\,\bar{q}$ or $\overline{pq}$ **s v pq**$\bar{s}$ cannot be summed to zero at the origin;

g. Process Rule 7—

g1. Translate vectors if a corresponding σ-point exist for a ι-point then σ is the simplification of ι;

g2. Any superpositions of parallel arrows in opposite directions represent equivalences,

g3. For equivalences, (a) drop the longer clause at either end of any doubleheaded arrow, (b) drop pairs, triples etc. of double-headed arrows which meet at a point in favor of the vector from that point to **O** and (c) drop a vector or clause in the target schema which is itself the resultant of any other two vectors;

h. Process rule 8—

h1. A simplification is complete if in the system which replaces the target schema no vectors or clauses are subsumed by others and no double-headed vectors remain.

Claim 5 (original) Apparatus for simplifying logical circuits, comprising:

a. a processing element configured to represent the logic of a logical circuit to be simplified as points and vectors in a vector space and to use the points and vectors to simplify the logic of the logical circuit to a simpler form.

Claim 6 (original) The apparatus of claim 5 in which the processing element is an optical computer.

Claim 7 (original) The apparatus of claim 5 in which the processing element is a digital computer.

Claim 8 (original) The apparatus of claim 1 in which the processing element is an colorimetric computer.

Claim 9 (original) The apparatus of claim 1 in which the processing element is an analog computer.

Claim 10 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be designed as points and vectors in a vector space and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler_ form and for designing the logical circuit using the simpler form.

Claim 11 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be manufactured as points and vectors in a vector space, and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form, and for using the simpler form to implement the logical circuit in hardware.

Claim 12 (original) A computer program product, comprising:

a. a memory element; and

b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit as points and vectors in a vector space, and for modifying the representation in a vector space using at least one process rule of a set of process rules to simplify the logic.